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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/877,720	06/08/2001	Christopher S. Moore	10519/32	8937

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EXAMINER	
LI, ZHUO H	

ART UNIT	PAPER NUMBER
2186	9

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/877,720	MOORE ET AL.
	Examiner	Art Unit
	Zhuo H Li	2186

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 June 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4-8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statements filed on October 3, 2001, January 28, 2002, October 7, 2002, March 4, 2003 and August 11, 2003 (Paper No. 4-8) are considered.

Double Patenting

2. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

3. Claims 1 and 8 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 18 of copending Application 09/877,719 filed on June 8, 2001. Although the conflicting claims are not identical, they are not patentably distinct from each other because all the claimed features of present Application 09/877, 720 are transparently found in copending Application 09/877, 719. Take an example of independent claim 1 between the present Application 09/877, 720 and the copending Application 09/877, 719 as following table:

Application 09/877, 720	Co-pending Application 09/877, 719
A method for storing and reading data in a write-once memory array, the method comprising:	A method for storing and reading a file system structure in a write-once memory array, the method comprising:
(a) inverting a plurality of bits representing data to be stored in a write-once memory array;	(a) inverting a plurality of bits representing a field system structure to be stored in a write-once memory array;
(b) storing the inverted plurality of bits in the memory array;	(b) storing the inverted plurality of bits in a write-once memory array;
(c) reading the inverted plurality of bits from the memory array; and	(c) reading the inverted plurality of bits from the memory array; and
(d) inverting the inverted plurality of bits read from the memory array.	(d) inverting the inverted plurality of bits read from the memory array.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

4. Claims 2-7, 9-11 and 13-16 are objected to because of the following informalities:

Regarding claims 2-7 and 13-16, "the invention of Claim" should be --the method of claim-- according to claims 1 and 12.

Regarding claims 9-11, "the invention of Claim" should be --the memory device of claim-- according to claim 8.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1 recites the limitation "a write-once memory array" and "the memory array" in line 3 and lines 5-7. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 2-7, are also rejected because of depending on claim 1, containing the same deficiency.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 1-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vining et al (US PAT. 6,377,526 hereinafter Vining) in view of de la Iglesia et al (US PAT. 6,490,703 hereinafter de la Iglesia).

Regarding claim 1, Vining discloses a method for storing and reading data in a write-once memory array, i.e., optical disk storing a plurality bits representing data (col. 1 lines 20-29 and col. 4 lines 61-66). Vining differs from the claimed invention in not specifically teaches the method further comprising inverting a plurality of bits representing data to be stored in a write-once memory array, storing the inverted plurality of bits in the memory array, reading the inverted plurality of bits from the memory array, and inverting the inverted plurality of bits read from the memory array. However de la Iglesia discloses a method for storing and reading data in a memory (206, figure 5), the method comprising inverting a plurality of bits representing data to be stored in the memory, storing the inverted plurality of bits in the memory array (col. 7 lines 19-42 and col. 7 line 55 through col. 8 line 44), i.e., the inputting data is inverted by the inversion generator (512, figure 5) before storing to the memory (206, figure 5), reading the inverted plurality of bits from the memory array, and inverting the inverted plurality of bits read

from the memory array, i.e., the stored inverted data is recovered by the inversion recovery (552, figure 5) before it transfer back to the processor (col. 7 lines 43-54 and col. 8 line 45 through col. 9 line 62). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the write-once memory array system of Vining in having the step of inverting a plurality of bits representing data to be stored in a write-once memory array, storing the inverted plurality of bits in the memory array, reading the inverted plurality of bits from the memory array, and inverting the inverted plurality of bits read from the memory array, as per teaching by the computer system of de la Iglesia, because it reduce the amount of power consumed by devices employing power-on logic state buses.

Regarding claim 2, de la Iglesia discloses a data storage device, i.e., processor (304, figure 5) coupled with a memory device (306, figure 5) comprising the memory array (col. 6 line 66 through col. 7 line 16 and col. 9 lines 18-62).

Regarding claim 4, de la Iglesia discloses a controller, i.e., memory interface (400, figure 5) of a memory device, i.e., memory (306, figure 5) comprising the memory array (col. 7 lines 19-42 and col. 7 line 55 through col. 8 line 44).

Regarding claim 5, de la Iglesia discloses a data-reading device, i.e., processor (304, figure 5) coupled with a memory device comprising the memory array (col. 6 line 66 through col. 7 line 16 and col. 9 lines 18-62).

Regarding claims 3 and 6, de la Iglesia discloses a data storage device, i.e., a processor (304, figure 5), i.e., data storage device, in the computer system (300, figure 5) enables inversion generation by sending, i.e., writing, signals to the inversion generator (512, figure 5) by determent whether the logic ones of data word comprise greater than forty nine percent of the

logic bits of the sixty four bit data word, and further inverting the data before it transfers to the memory device (306, figure 5) and (figure 8 and col. 9 lines 18-62), and a data reading device, i.e., a processor (304, figure 5) is able to read the inverted data out from the memory (306, figure 5) via the inversion recovery (522, figure 5) and (col. 9 lines 18-62). The difference between de la Iglesia and the claims is the claims specifically recite both the data storage device and the data reading device comprise a device selected from the group consisting of a digital audio player, a digital audio book, an electronic book, a digital camera, a game player, a general-purpose computer, a personal digital assistant, a portable telephone, a printer, and a projector. However, having various of data reading devices do not have a disclosed purpose nor are this data reading devices to overcome any deficiencies in the prior art. As such, data reading device and data storage device would be have been any of devices that capable to general a memory operation. In addition, since de la Iglesia discloses a processor is able to general memory access operation, such as reading the stored data and updating a stored data in the memory as mention above and (col. 1 lines 9-29). Accordingly, it would have been an obvious matter of design choice to utilize the system of de la Iglesia wherein the data reading device is a processor, as disclosed supra, since applicants have not discloses that a device selected from the group consisting of a digital audio player, a digital audio book, an electronic book, a digital camera, a game player, a general-purpose computer, a personal digital assistant, a portable telephone, a printer, and a projector, as opposed to other special functionaries, overcomes a deficiency in the prior art or is for any stated purpose.

Regarding claim 7, de la Iglesia discloses a controller, i.e., memory interface (400, figure 5) of a memory device comprising the memory array (figure 5 and col. 7 line 19 through col. 8 line 62).

Regarding claim 8, Vining discloses a memory device, i.e., optical drive (100, figure 1) comprising a write-once memory array, i.e., optical disk, storing a plurality of bits representing data (col. 1 lines 20-29 and col. 4 lines 61-66), a controller (figure 1) coupled with the memory array. Vining differs from the claimed invention in not specifically teaches the memory controller is operate to invert the plurality of bits representing the data when the plurality of bits is read from the memory array. However, de la Iglesia teaches the computer system (300, figure 5) comprising a memory controller, i.e., memory interface (400, figure 5) coupled to the memory device (306, figure 5) wherein the memory controller further comprising a inverted recovery unit (552, figure 5) to recovery the inverted data become original state before it transfers back to the processor (304, figure 4) from the memory (col. 7 lines 19-54 and col. 8 line 45 through col. 9 line 62). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the controller of Vining is able to perform an memory operation to invert the plurality of bits representing the data when the plurality of bits is read from the memory array, as per teaching by the memory controller of de la Iglesia, because it reduce the amount of power consumed by devices employing power-on logic state buses.

Regarding claim 9, de la Iglesia discloses the controller is further operative to invert a plurality of bits representing data to be stored in the memory array via the inversion generator unit (512, figure 5) and (col. 7 line 19 through col. 8 line 44).

Regarding claim 10, de la Iglesia discloses the memory device comprise a solid-state memory device (col. 7 lines 3-16).

Regarding claim 11, Vining discloses the memory device comprises an optical memory device (figure 1).

Regarding claim 12, Vining discloses a method for redefining an initial, un-programmed digital state of a write-once memory array, i.e., optical disk (figure 1), the method comprising providing a memory array comprising a plurality of write-once memory cells, i.e., memory sector (col. 4 lines 61-66), the plurality of write-once memory cells comprising an initial, un-programmed digital state that can be switched to an alternative, programmed digital state (col. 5 lines 37-64 and col. 6 line 18 through col. 9 line 38), i.e., the write-once memory can able to program as erasable write-once memory, and redefining the initial, un-programmed digital state, i.e., logic one or logic zero, of the plurality of write-once memory cells as the alternative. Vining differs from the claimed invention in not specifically teaches programmed digital state by storing bits in the plurality of write-once memory cells in an inverted form. However, de la Iglesia disclose a computer system (300, figure 5) comprising a memory controller, i.e., memory interfacing in between a processor (304, figure 5) and memory device (306, figure 5), wherein the memory controller transferring the data read from and write to the memory device as upon requested from the processor, in addition, the memory controller further comprising a inversion generator unit (512, figure 5) which inverting the data to be stored in the memory device and comprising a inversion recovery unit (522, figure 5) which recovered the inverted data become the original state before the data transfer back to the processor from the memory (col. 7 line 19 through col. 9 line 62). Therefore, it would have been obvious to a person of ordinary skill in the

art at the time the invention was made to modify Vining in having step of programmed digital state by storing bits in the plurality of write-once memory cells in an inverted form, as per teaching by the computer system of de la Iglesia, because it reduce the amount of power consumed by devices employing power-on logic state buses.

Regarding claim 13, de la Iglesia discloses the initial, un-programmed digital state comprises Logic 1, and wherein the alternative, programmed digital state comprise Logic 0 (col. 1 lines 30-40 and col. 7 line 19 through col. 8 line 44).

Regarding claim 14, Vining discloses the initial, un-programmed digital state comprises Logic 0, and wherein the alternative, programmed digital state comprises Logic 1 (col. 1 lines 20-29 and col. 4 lines 61-66 and col. 5 lines 15-64).

Regarding claims 15-16, Although Vining does not clearly discloses the memory array comprising a three-dimensional and/or two -dimensional memory array, Vining teaches the write-once memory disk, i.e., optical disk comprising a plurality of sectors wherein each sector including data bits, i.e., user data, flag field and SWF field which both contains value (col. 3 lines 25-56 and col. 5 lines 57-64). Thus, one skill in the art recognizes the write-once memory disk of Vining is a three-dimensional and/or two -dimensional memory arrays.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Cozart et al. Discloses ROM, i.e. write-once memory mapping and inversion apparatus and method wherein the ROM data may be selectively inverted to decrease energy dissipation (abstract).

Rivest et al. (US PAT. 4,691,299) discloses method and apparatus for reusing non-erasable memory media (abstract).

Sassa et al. (US PAT. 6,345,333) discloses method and apparatus for reverse rewriting to prevents a damage concentration caused by a data erase/write-in to a particular cell, so as to increase a service life of a flash memory (col. 1 line 49 through col. 2 line 43).

Norman (US PAT. 6,073,208) discloses method and apparatus for reducing programming cycles for multistate memory system (abstract).

10. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 746-7238

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The

examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li

March 19, 2004

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100